

FPGA

Upduino 3.1 demo, place and route, timing report

Taeho Lee

August, 2026

1 Demo target

The demo target is the Upduino 3.1 (iCE40UP5K-SG48), a low-cost board with an onboard 12 MHz oscillator and 8 MB PSRAM. The whole toolchain is open source: Yosys for synthesis, nextpnr-ice40 for place and route, icepack for the bitstream, and icetime for timing analysis.

The demo top module registers the decode on the board clock, so the one-cycle latency and the timing closure are measurable with a real clock:

Signal	Source	Destination
clk	pin 20, onboard 12 MHz oscillator	global clock
code[15:0]	GPIO switch module	decoder input
i[4:0], m[4:0], f[4:0]	decoder output	LED groups
led_valid	~valid, range check	onboard green LED (negative logic, lights on valid code points)

Pin constraints are verified against the Upduino v3.1 reference PCF from the icestudio project.

2 Place and route flow

```
synth_demo.ys    -> out/tagma_demo_top.json    (Yosys, iCE40)
nextpnr-ice40    -> out/tagma_demo_top.asc      (place and route, --freq 12)
icepack          -> out/tagma_demo_top.bin      (bitstream)
icetime          -> reports/icetime.txt        (timing report)
```

3 Timing results

Metric	shift-subtract (naive)	multiply-shift (current)
ICESTORM_LC	177 / 5280 (3%)	255 / 5280 (4%)
SB_IO	33 / 39	33 / 39
SB_GB	1 / 8	1 / 8
Logic levels	72	33
Critical path	115.90 ns	59.55 ns
Fmax	8.63 MHz	16.79 MHz

The multiply-shift version closes the 12 MHz board clock with margin. The bitstream is generated and the design is ready for board bring-up.

4 Board bring-up

The remaining step is physical: program the bitstream, wire a DIP switch module and LED modules to the GPIO pins in the constraint file, and capture the demo. The onboard 8 MB PSRAM also covers the RAM-attached test device question: a chthon segment store can be exercised on the same board.